



REPLACEMENT SHEET

Application No.: 10/606,419

Title: System and Method for Guiding and Optimizing Formal Verification for a Circuit Design

Inventor(s): Vigyan Singhal et al.

Atty. Docket No.: 24006-08742

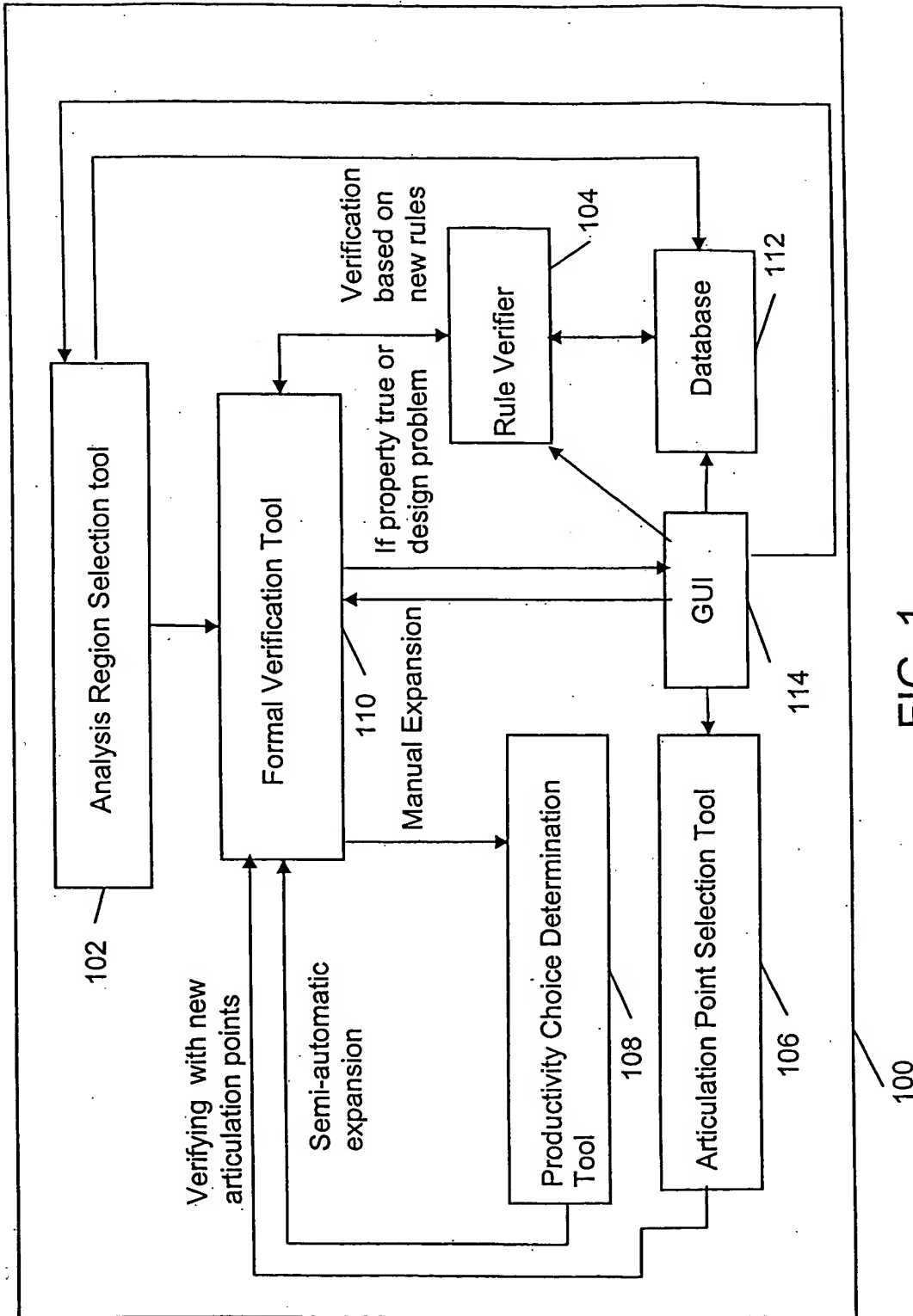


FIG. 1

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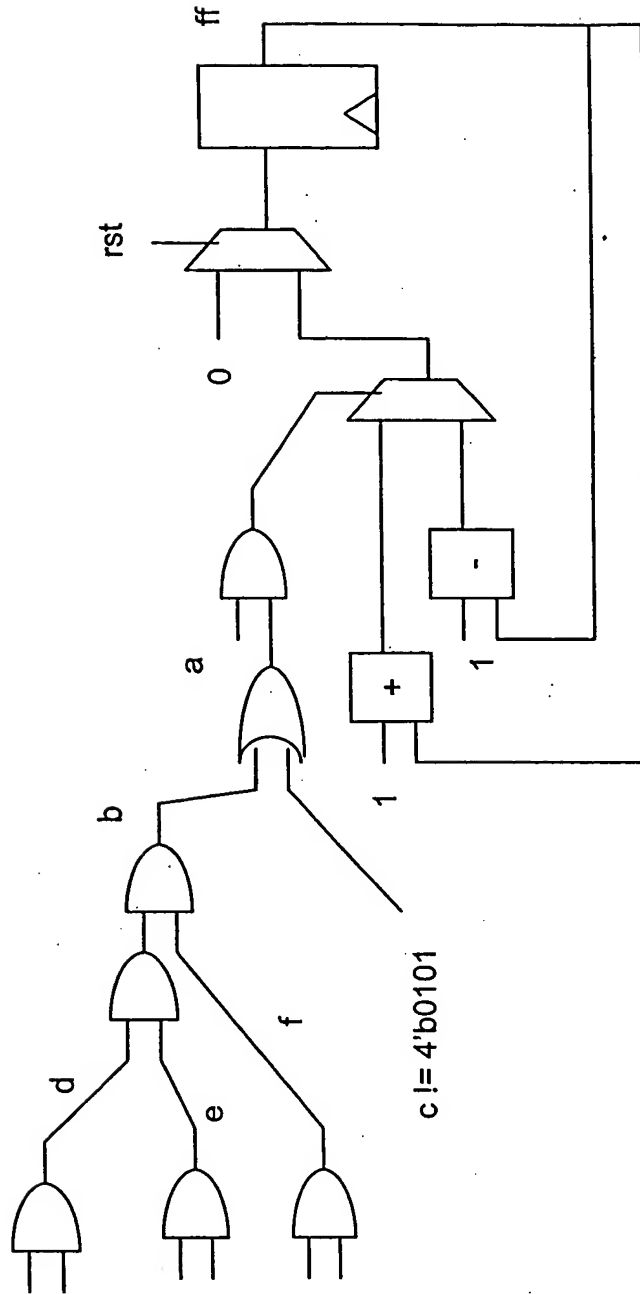


FIG. 2

Atty. Docket No.: 24006-08742



FIG. 3

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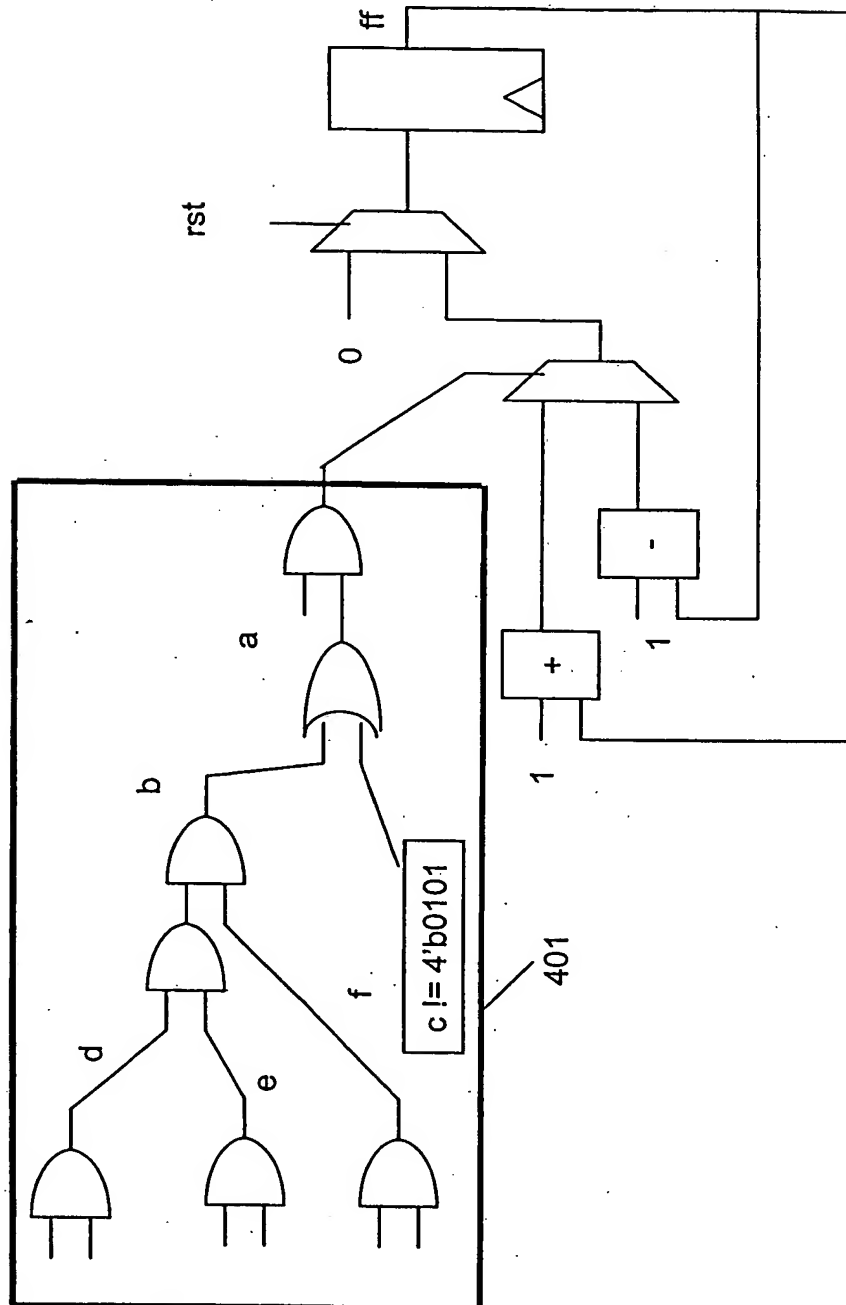


FIG. 4

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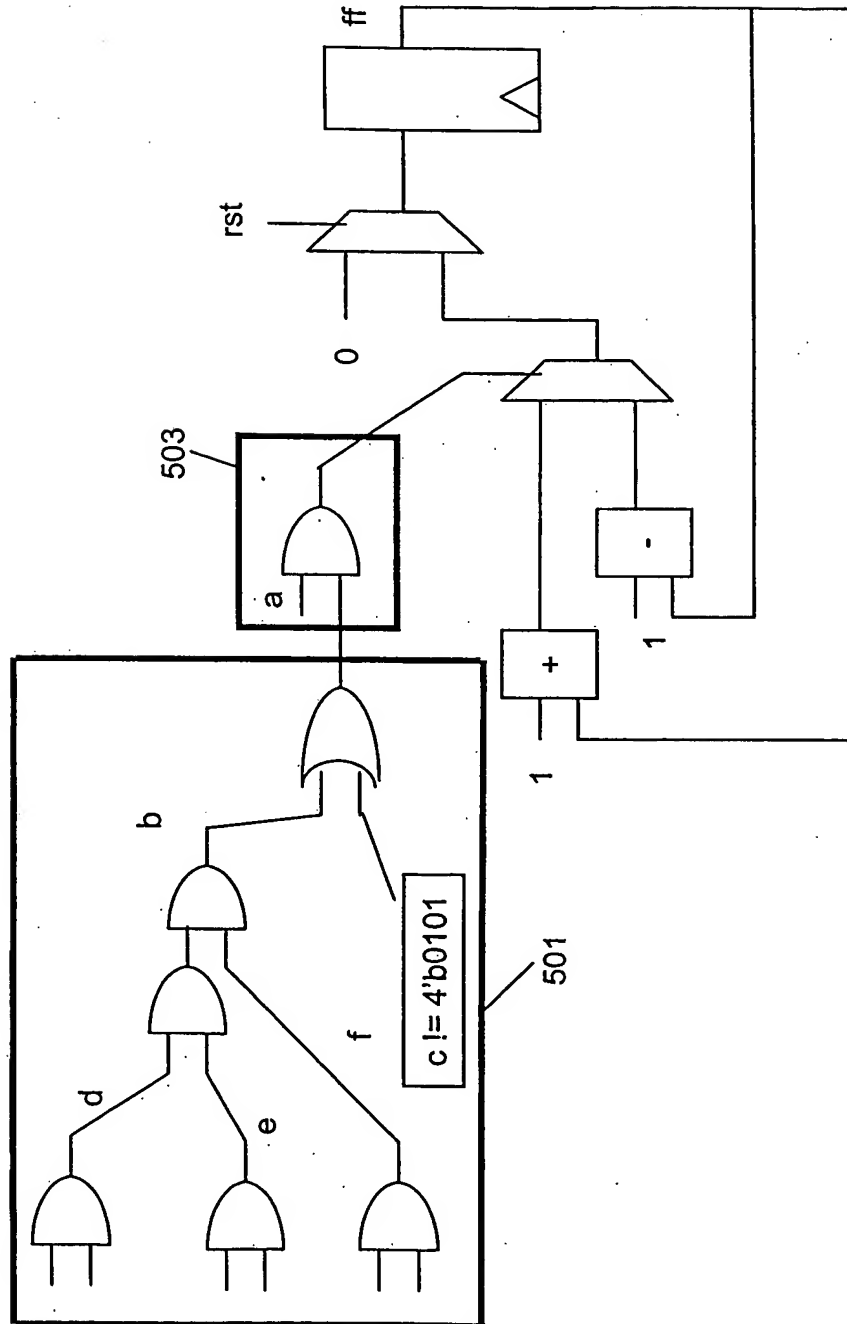


FIG. 5

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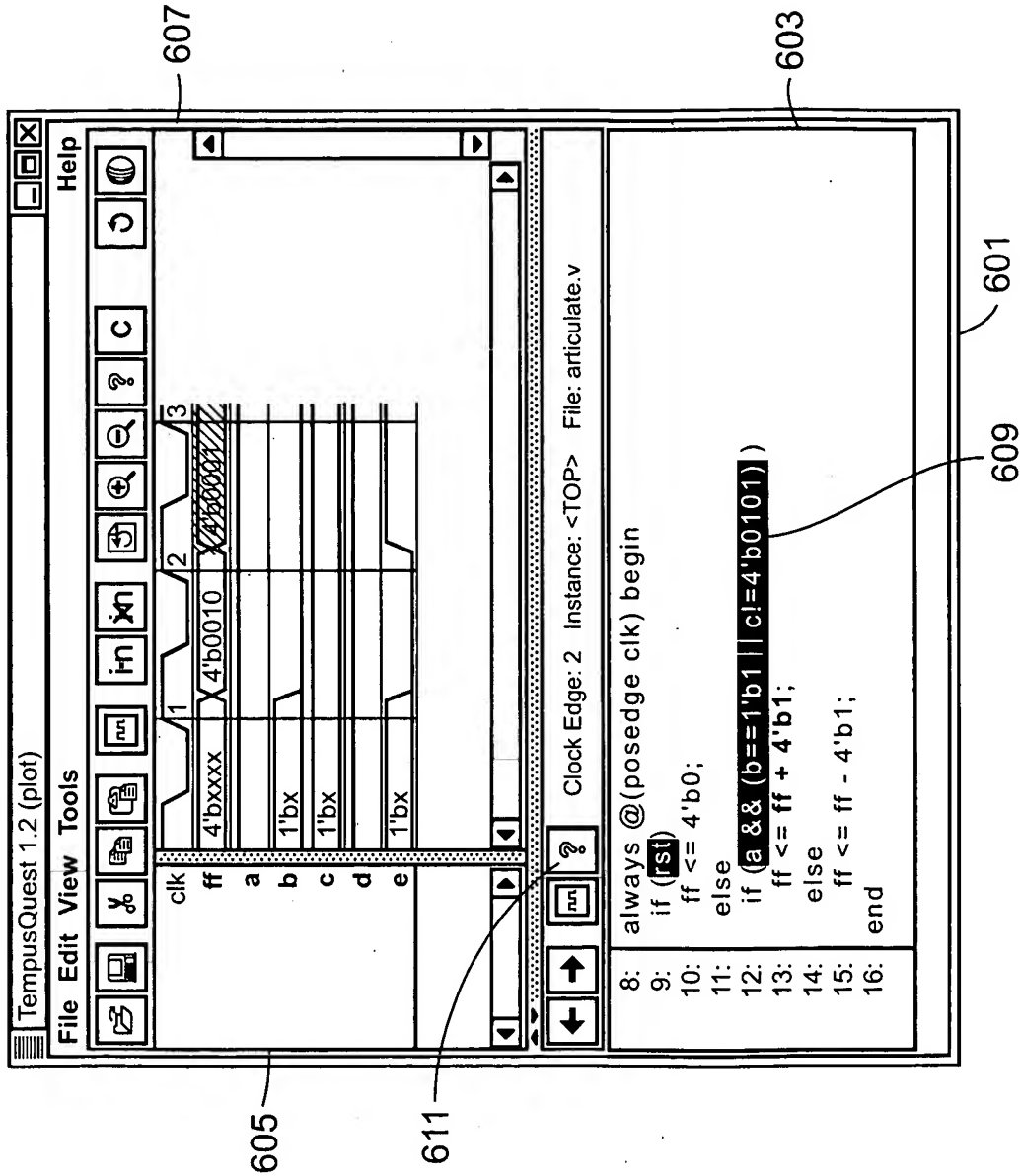


FIG. 6

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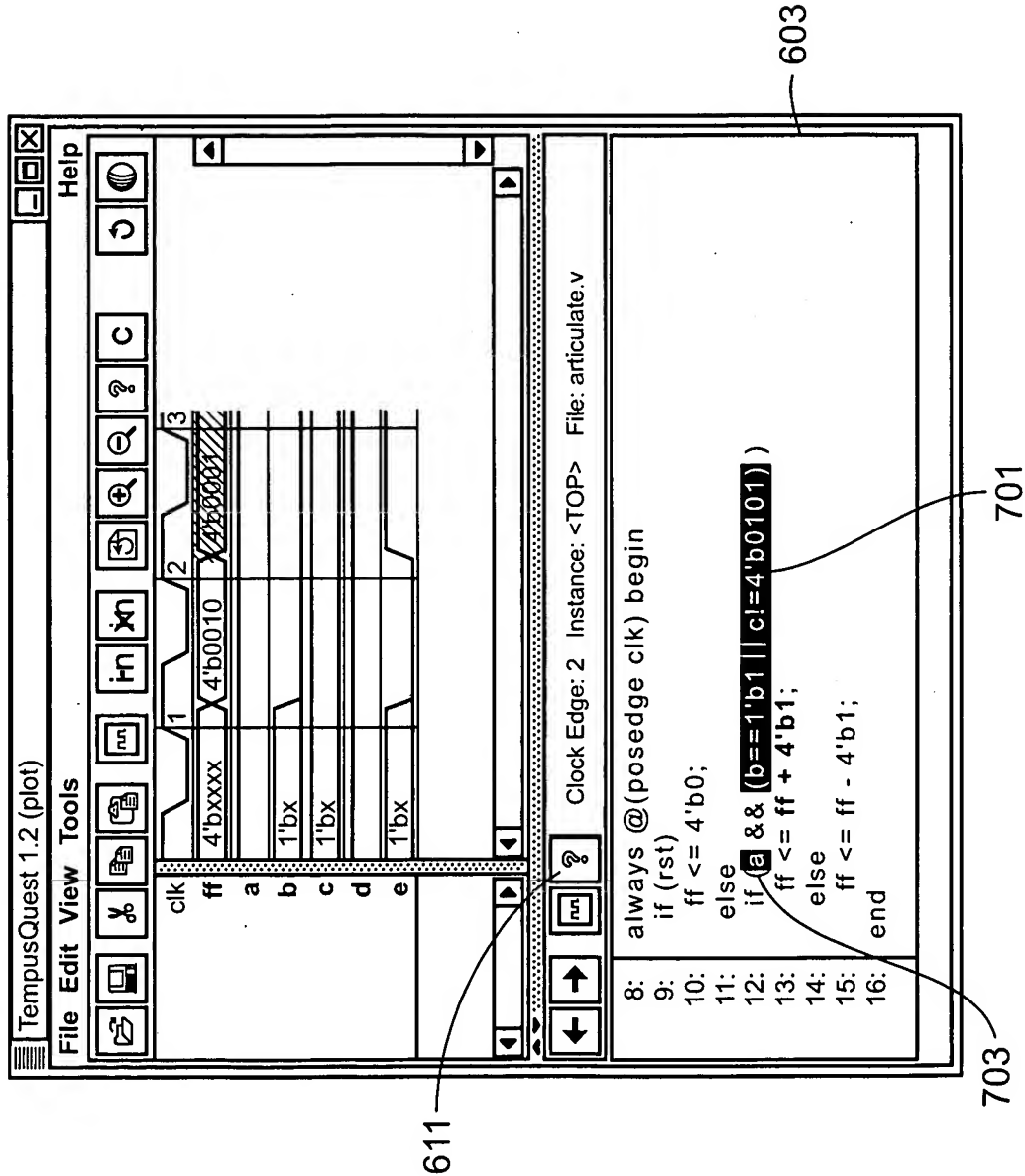


FIG. 7

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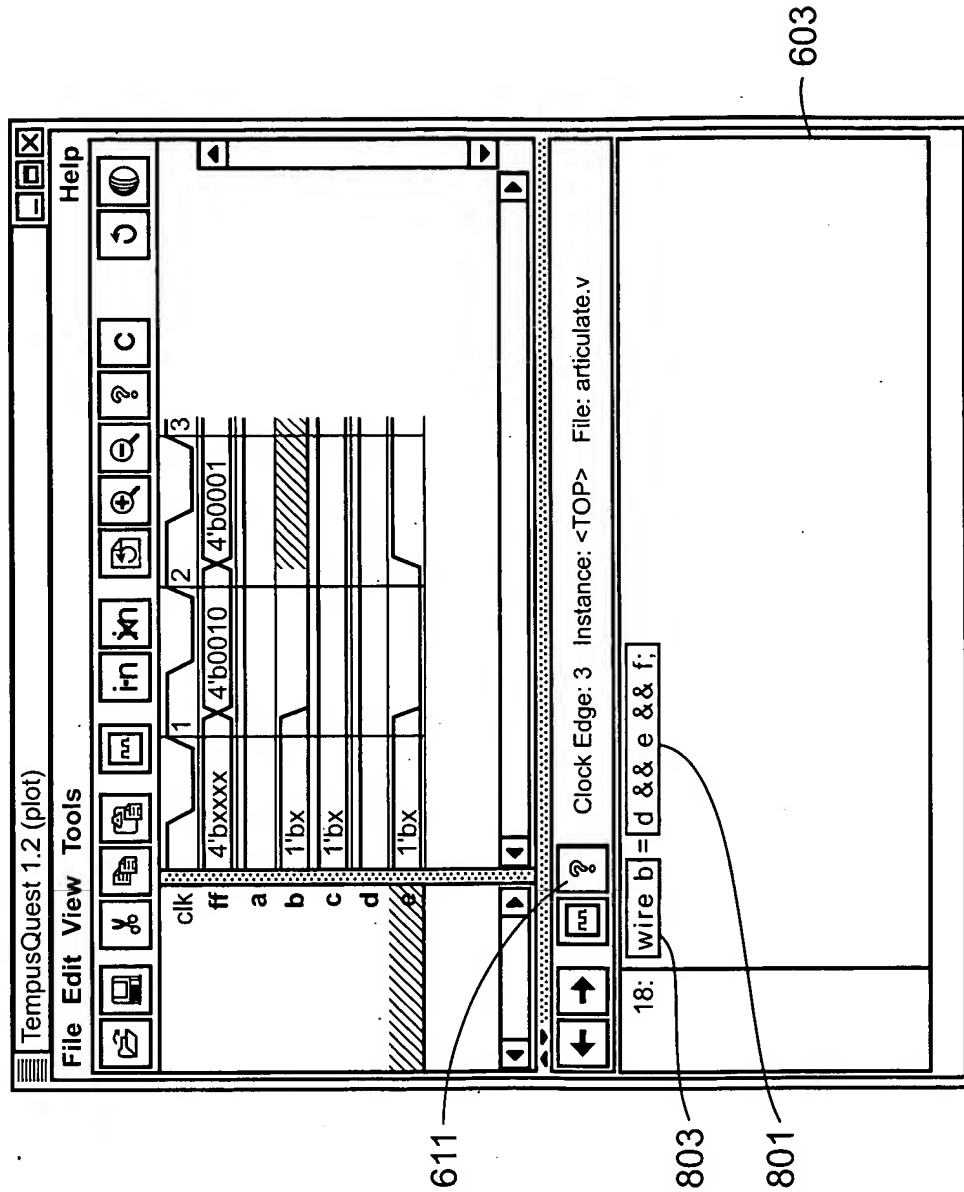


FIG. 8

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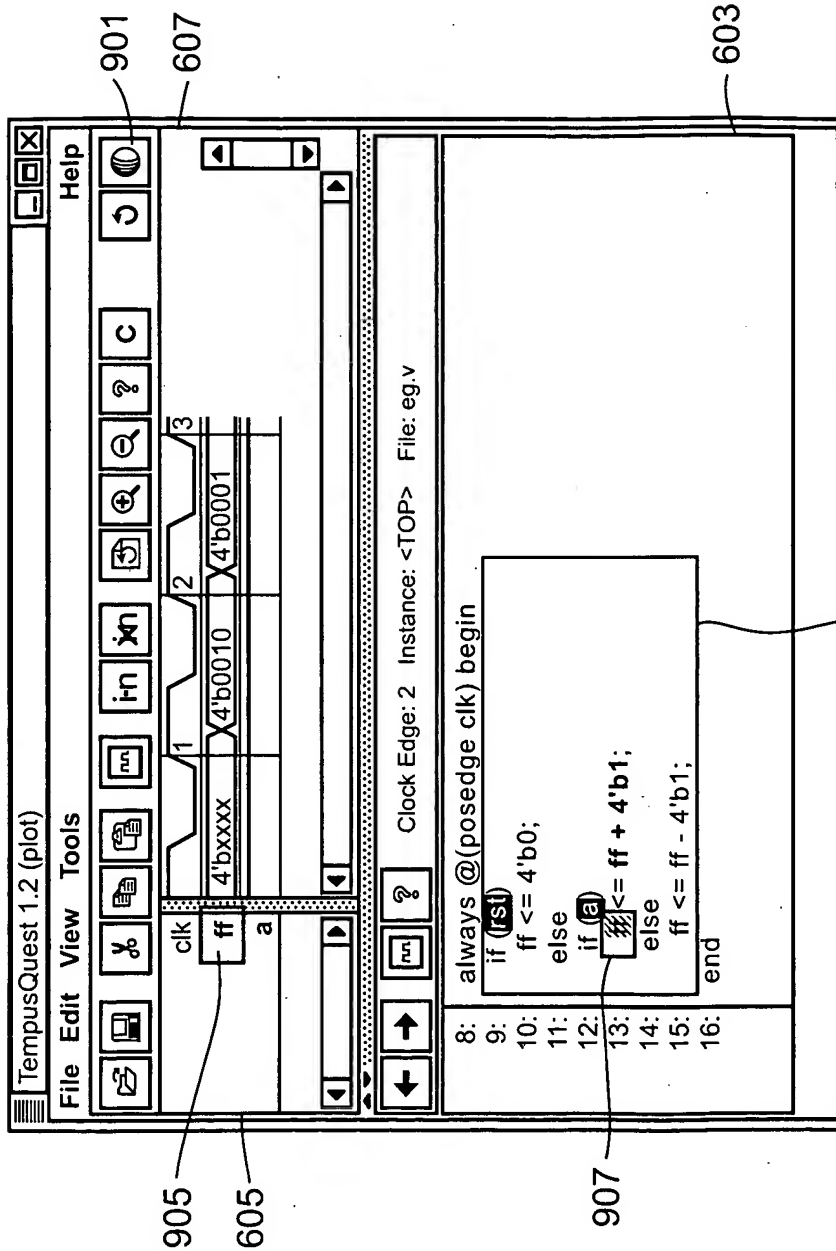


FIG. 9

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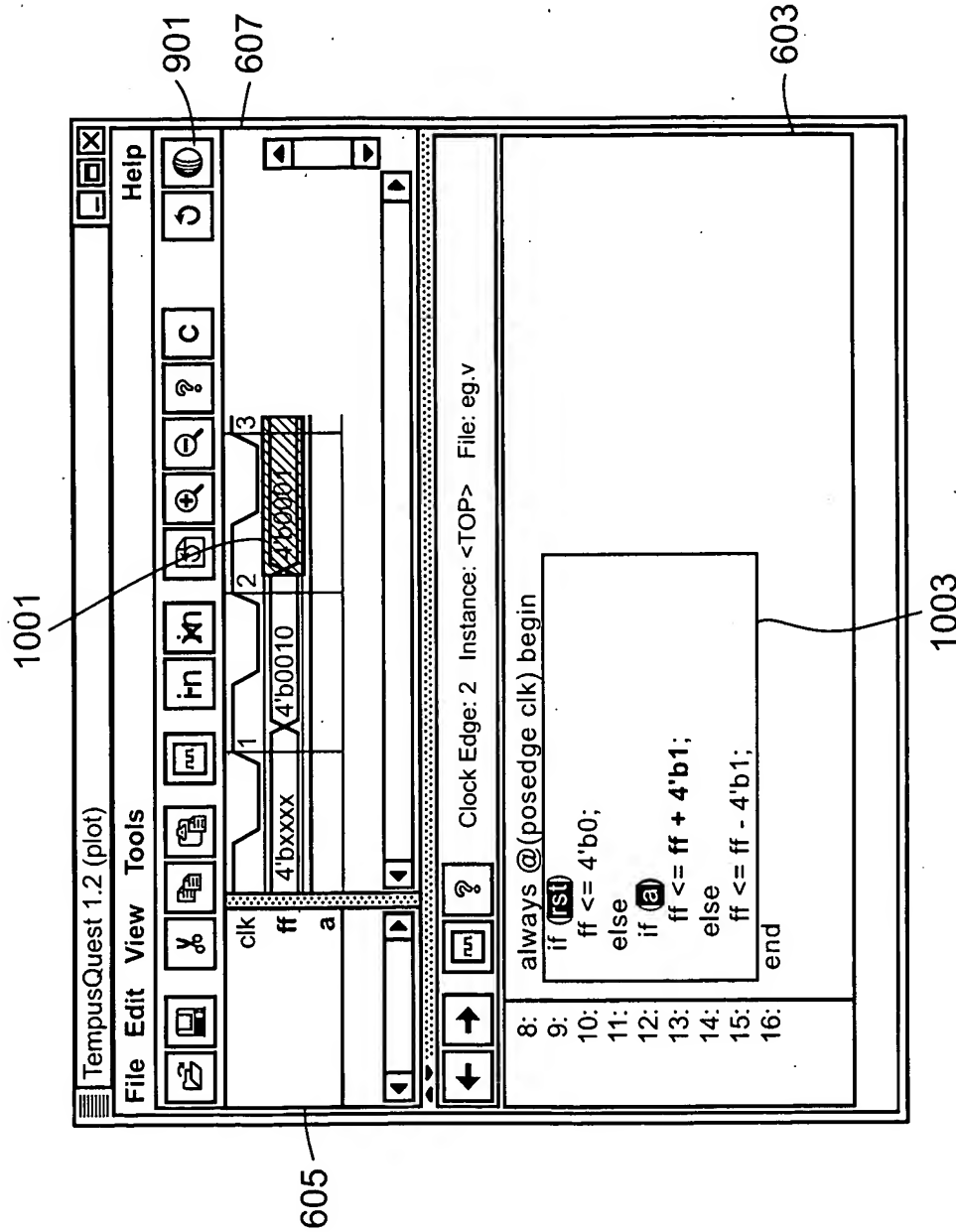


FIG. 10

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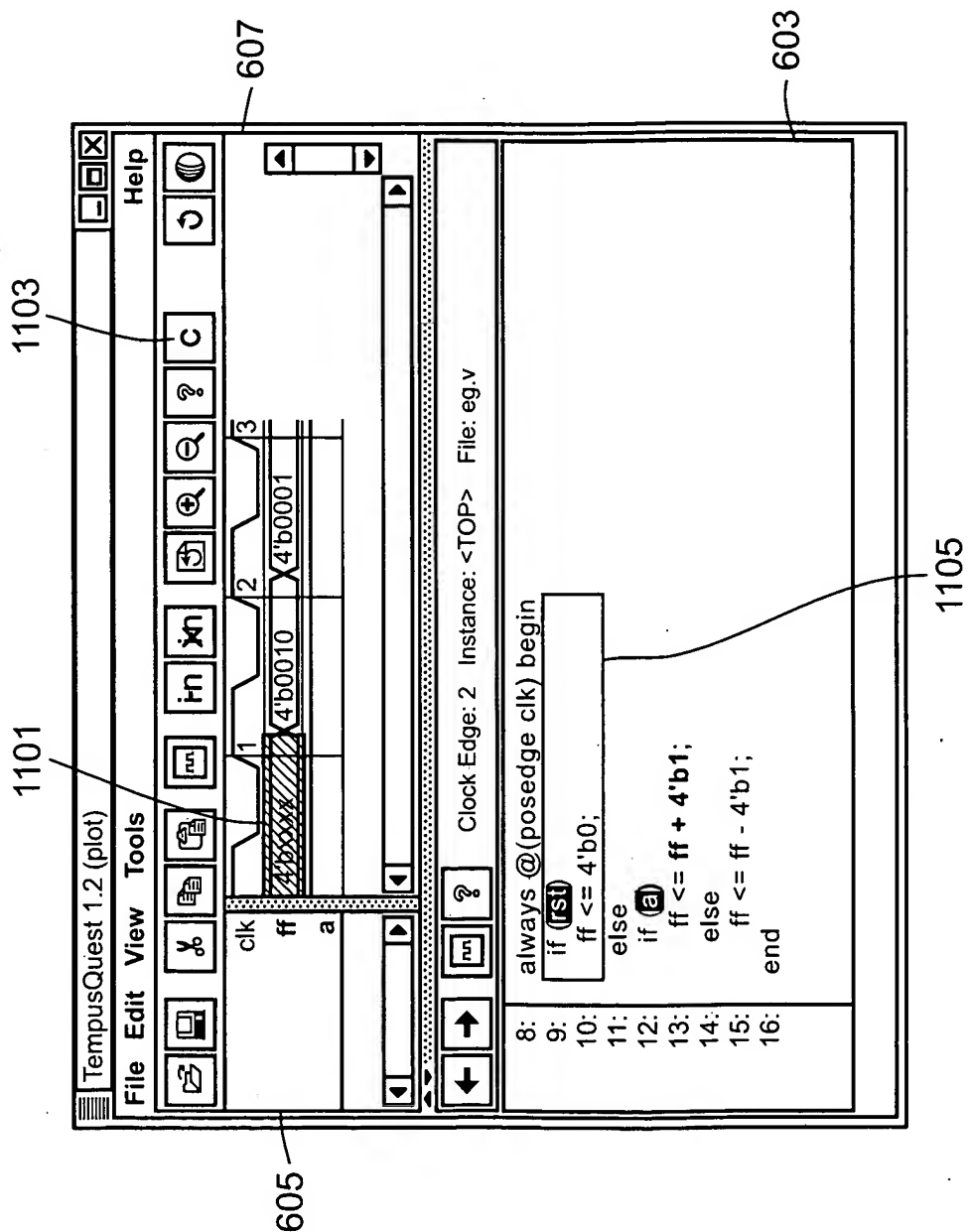
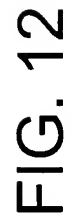


FIG. 11

Atty. Docket No.: 24006-08742



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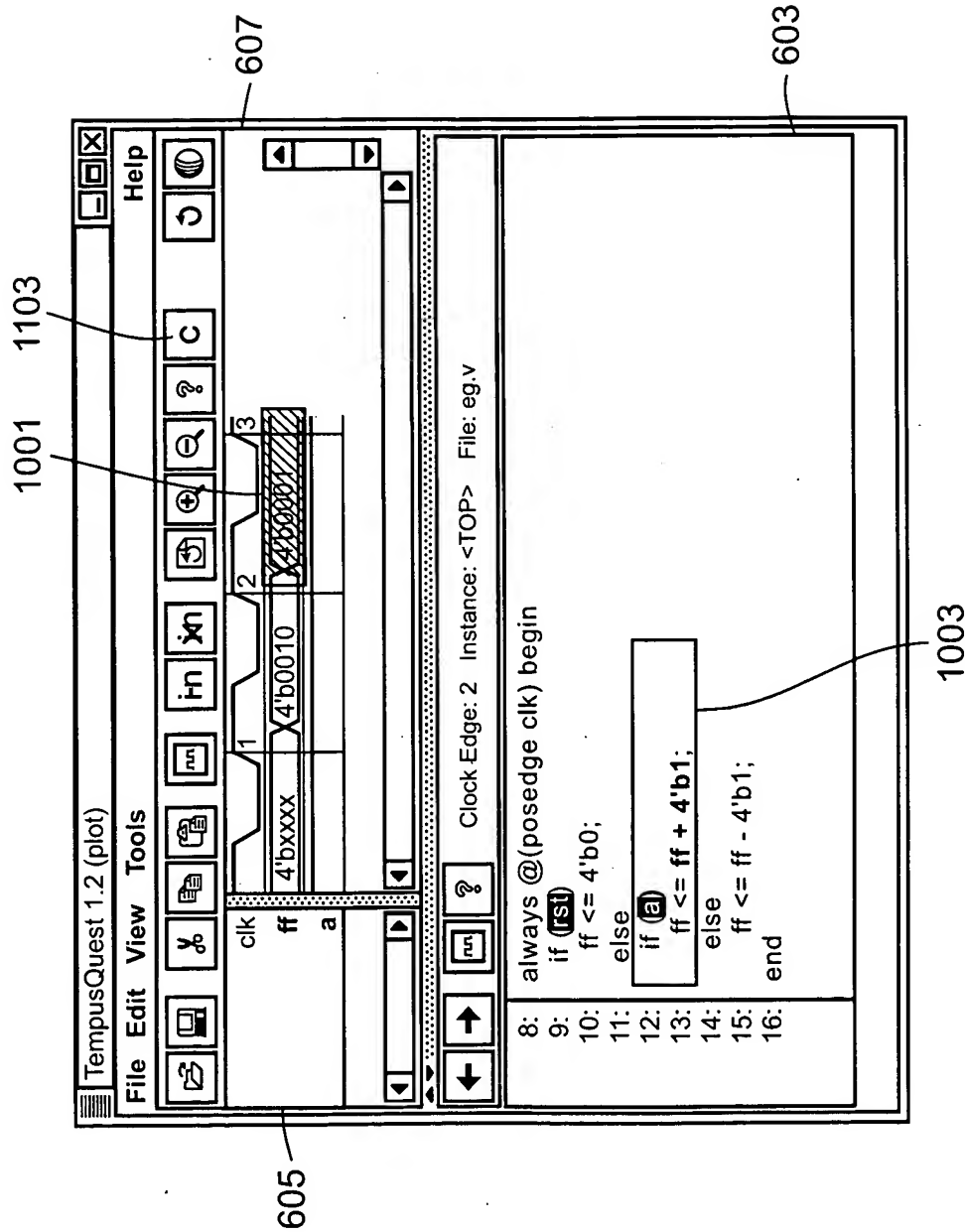


FIG. 13

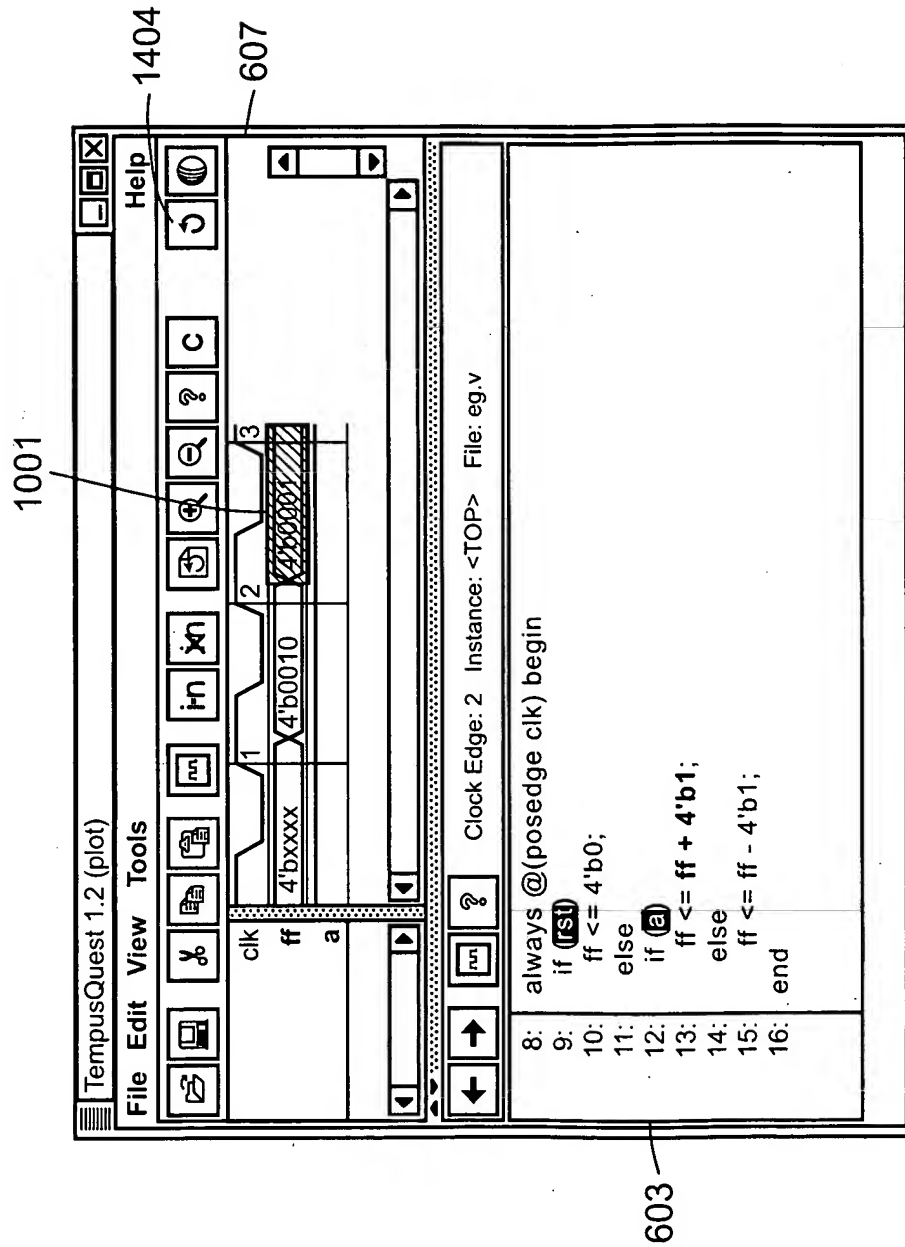


FIG. 14

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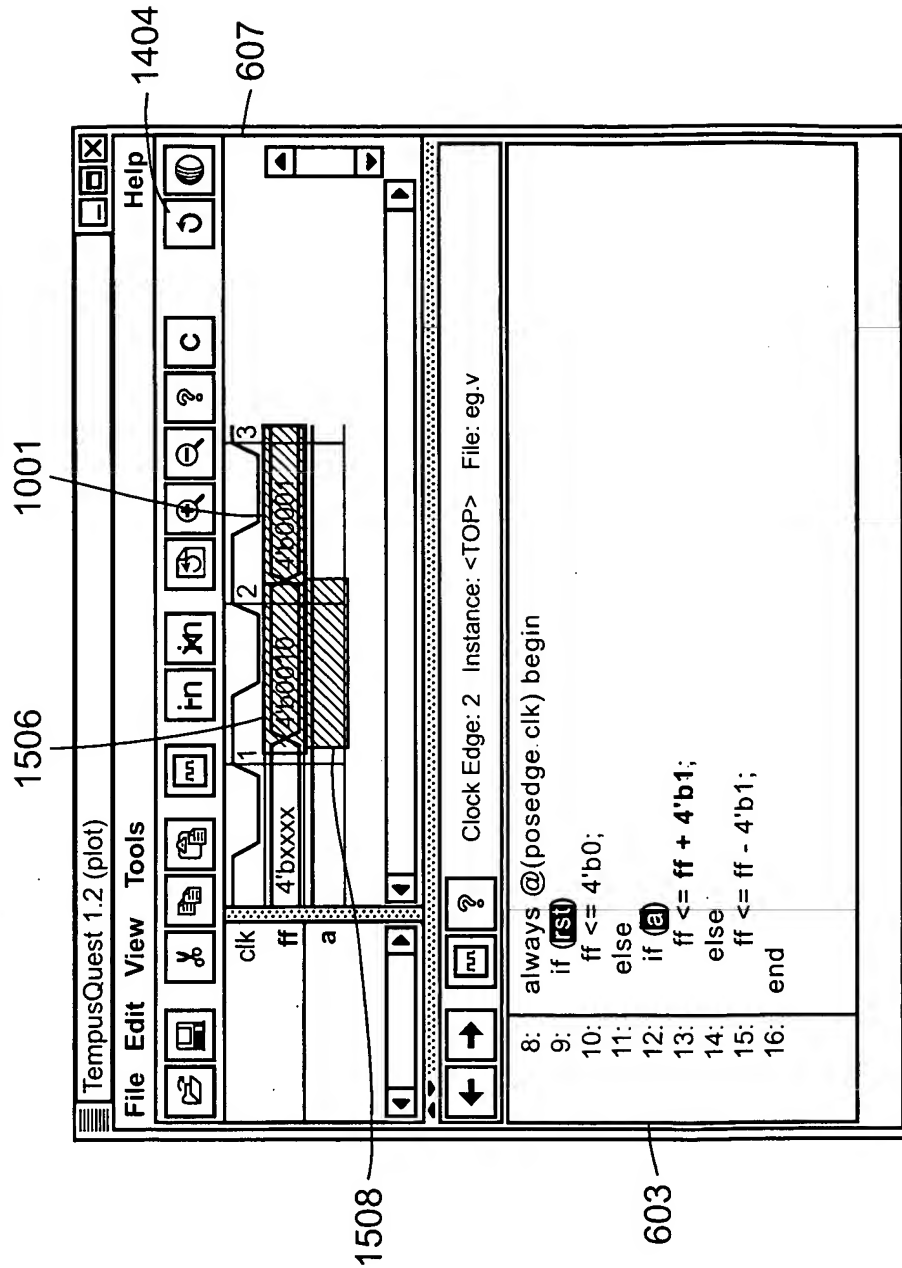


FIG. 15

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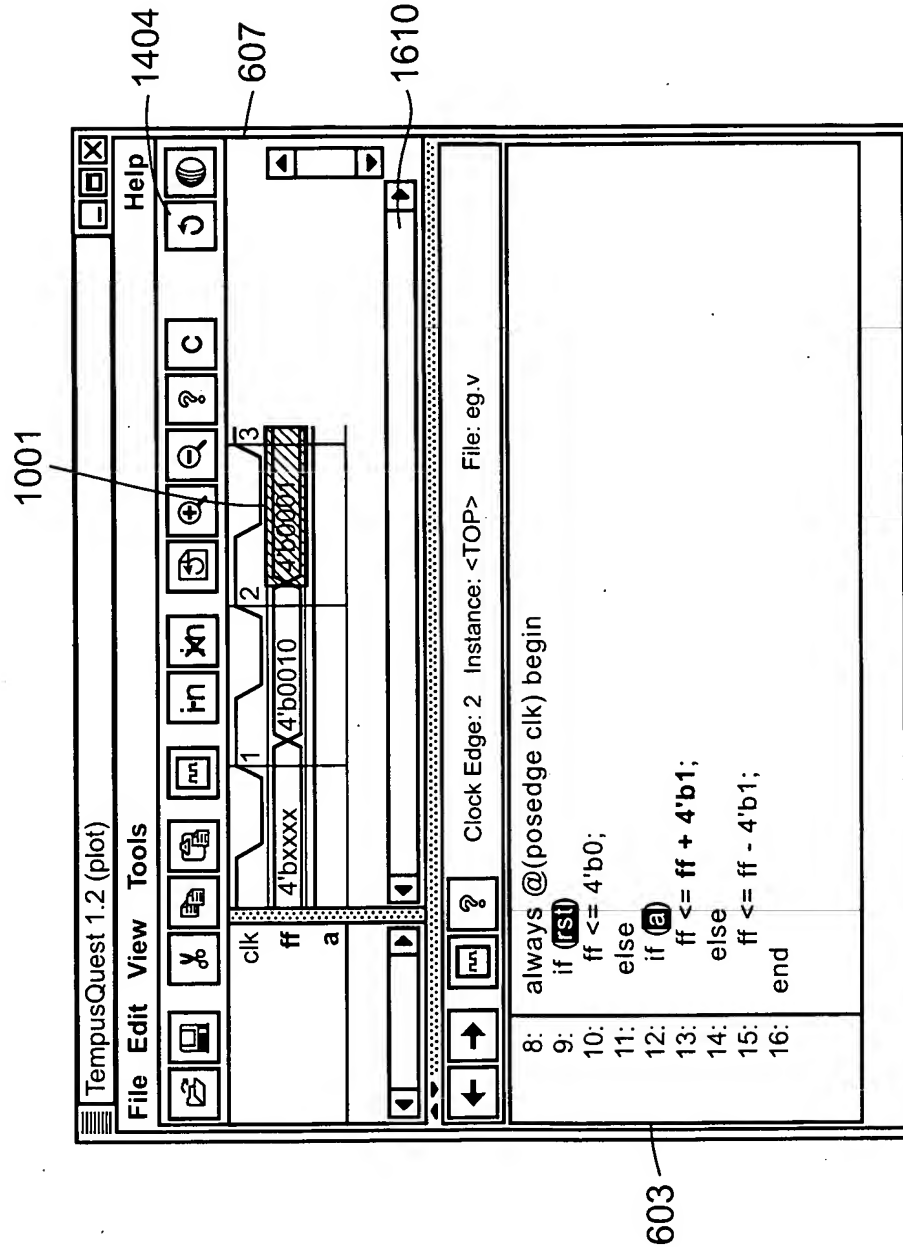


FIG. 16